Final Expansion 3 Programmers Guide

Version 1.0

Copyright Information

Version Information

Version	Date	Changes
1.0	2025-04-26	Initial version

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Contents

Introduction

This guide covers various aspects of how to write programs to make use of the memory expansion capabilities of the Final Expansion 3 cartridge for the VIC-20. It does not cover details of the emulated disk drive as this is identical to standard SD2IEC devices.

For general usage of the FE3 see the separate “Final Expansion 3 Users Guide.”

Where to Get Help

The on-line forum Denial, http://sleepingelephant.com/denial/, is a community of VIC-20 users. They may be able to provide information and suggestions but cannot be expected to resolve your specific problems.

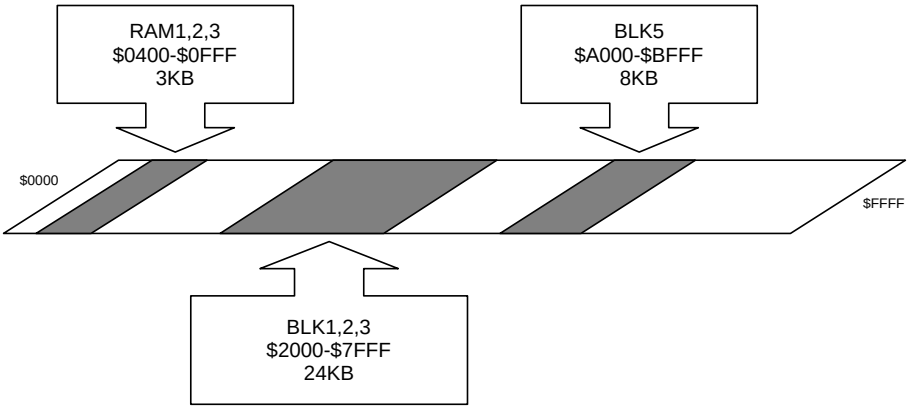
VIC-20 Memory Map

This section gives an overview of how memory is laid out in the VIC-20.

An unexpanded system contains:

- 5KB of Random Access Memory (RAM)
- 20KB of Read Only Memory (ROM)
- 2KB of Input/Output (IO) register space

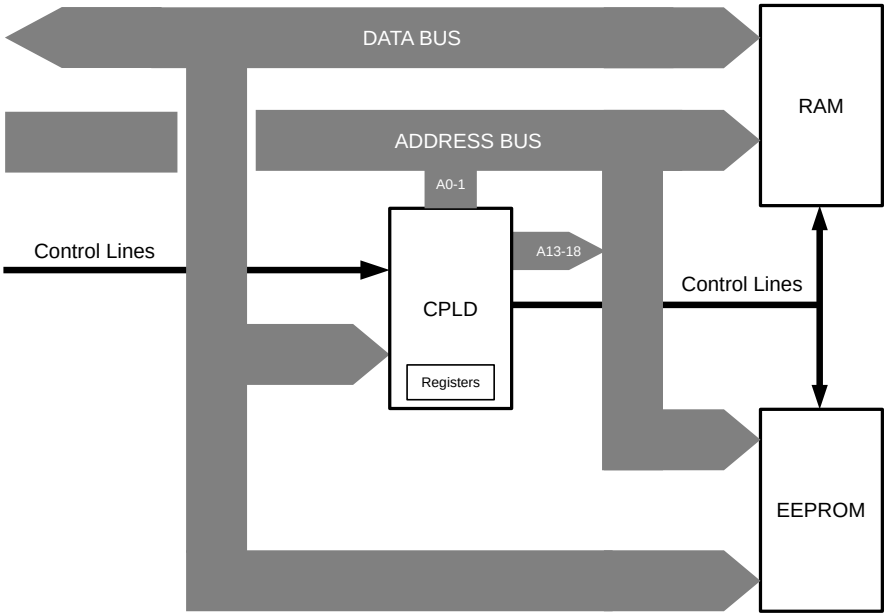
The expansion port provides various pins to allow memory to be added at addresses outside of these areas. There are three regions available for expansion.



The FE3 can be configured to present memory into any or all of these regions.

FE3 Block Diagram

The following diagram shows the main components of the FE3 and how they connect to the various lines of the VIC-20 expansion port.



RAM

Read/write memory is provided by a 4Mbit static random access memory (SRAM) device configured as 512Kb x 8bit.

EEPROM

Persistent memory is provided by a 4Mbit electrically erasable programmable read only memory (EEPROM) device configured as 512Kb x 8bit.

CPLD

The custom, flexible memory expansion capabilities of the FE3 are controlled by a complex programmable logic device (CPLD).

It is configured by software running on the VIC-20 through a pair of 8-bit

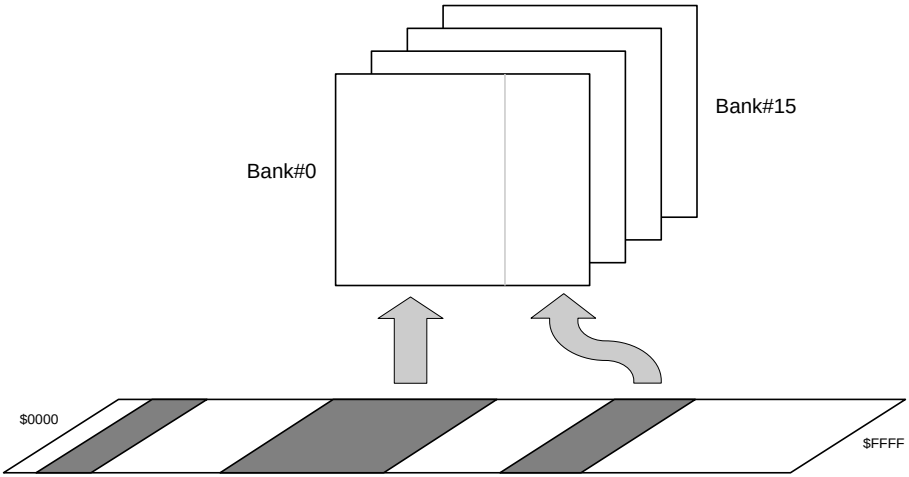
registers which can be read and written to.

The CPLD generates additional address lines to allow access to the full address range of the memory devices. It also selects which device is active at any time.

FE3 Memory Addressing

Each of the RAM and EEPROM devices have separate linear address spaces covering 512KB. To select any specific byte in one requires 19 address lines. Excluding the RAM1,2,3 area the expansion port can only access a total of 32KB (BLK1,2,3,5 each of 8KB).

The CPLD is responsible for generating the extra address lines, it does this by using an index called a **bank** which is 4 bits wide. Combining the bank with an offset for each of the four 8KB blocks creates a linear address for either of the memory devices.



The value used for the bank depends on the current **mode** the FE3 is configured with.

The RAM1,2,3 area, when present, always maps to the first 3KB of Bank 0 of the RAM device. This means in some modes it is aliased with the first 3KB in BLK1.

Bank Usage

In normal operation the following banks are used for specific purposes.

Bank	RAM	EEPROM
0	Memory in RAM1,2,3	FE3 firmware & flash catalogue
1	Memory in BLK1,2,3,5	Flash packages
2+	Unused	Flash packages

RAM banks 2 and higher are available for application use.

Registers

There are two registers that manage behaviour of the FE3

1. Mode register – current mode and bank
2. Resource register – enabled blocks and other configuration

These registers are memory-mapped in the $\overline{\text{IO3}}$ region, their addresses are

- $9C02 – mode register
- $9C03 – resource register

The top 3 bits of the mode register determine the current mode. The other 5 bits have different effects, depending on the mode.

The bits of the resource register have the following functions

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
e	*a*	*b*	*5*	*3*	*2*	*1*	*r*

- *e* – disable registers (0=enable registers, 1=disable registers)
- *a* – invert A14

- *b* – invert A13
- *5* – disable BLK5
- *3* – disable BLK3
- *2* – disable BLK2
- *1* – disable BLK1
- *r* – disable RAM1,2,3

Warning! Once registers have been disabled by setting b7 of the resource register they can only be re-enabled by a cartridge reset.

Modes

The FE3 can operate in one of 7 different modes. Each mode defines, for read and write operations separately

- which device to target
- which bank to target

The target device can be either

- a constant
- a choice of device depending on a block-specific value in the bottom bits of the mode register

The target bank can be either

- a constant
- a choice of two banks depending on a block-specific value in the bottom bits of the mode register
- a value in the bottom bits of the mode register

This gives modes the flexibility to choose between addressing any location in a given device or allowing different banks and/or devices at different physical memory addresses.

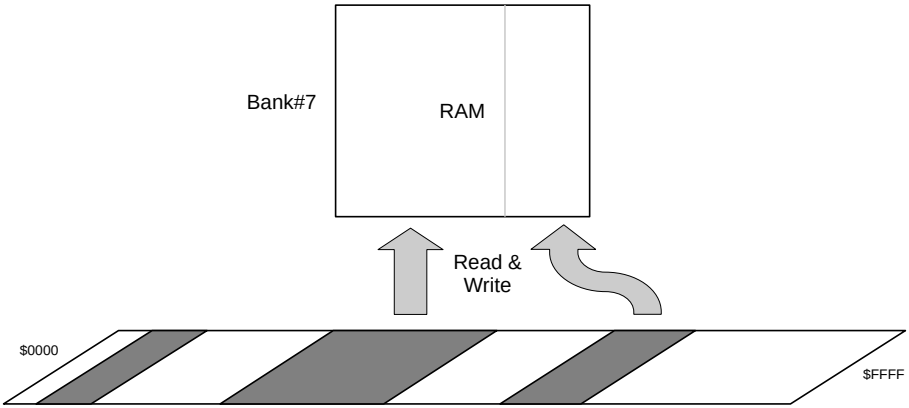
Modes which are of interest to general application writers are introduced

first. Later ones are of use for specialized purposes (such as replacement firmware).

Super RAM Mode

This mode is selected by setting the top 3 bits of the mode register to %101. All reads and writes are targeted at the RAM device and the bank is determined by the bottom 4 bits of the mode register.

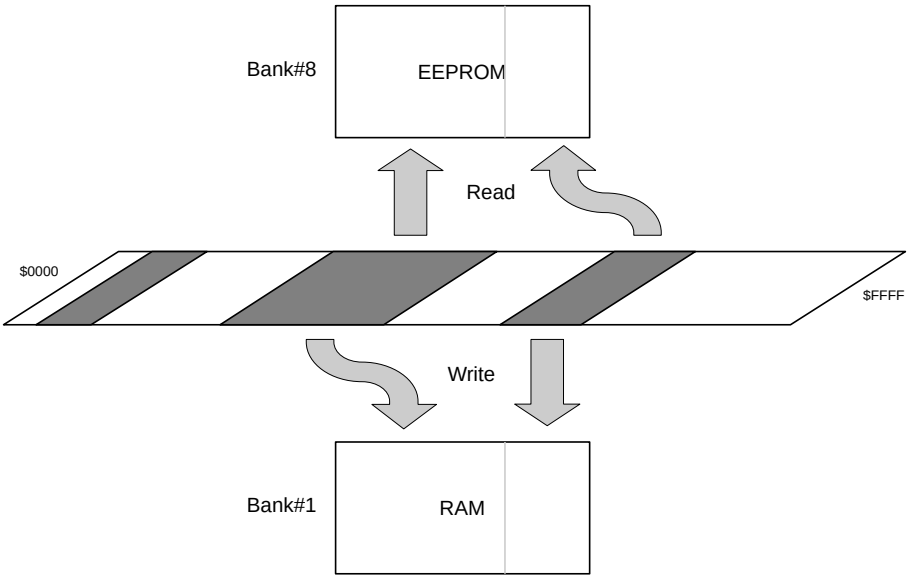
For example, setting the mode register to %10100111 selects bank 7 for both reads and writes in all blocks.



Super ROM Mode

This mode is selected by setting the top 3 bits of the mode register to %010. All reads are targeted at the EEPROM device and the bank is determined by the bottom 4 bits of the mode register. All writes are targeted at bank 1 of the RAM device.

For example, setting the mode register to %01001000 selects bank 8 for reads and bank 1 for writes in all blocks.



RAM1 Mode

This mode is selected by setting the top 3 bits of the mode register to %100. All reads are targeted at bank 1 of the RAM device, writes go to either bank 1 or 2 depending on the value of a block-specific bit in the bottom of the mode register and the address the block is in.

Bit	Block	Effect
4	BLK5	0 – bank 1, 1 – bank 2
3	BLK3	0 – bank 1, 1 – bank 2
2	BLK2	0 – bank 1, 1 – bank 2
1	BLK1	0 – bank 1, 1 – bank 2

Bit 0 of the mode register controls write access to RAM1,2,3. If the bit is set the region is write-protected.

For example, setting the mode register to %10010100 selects bank 2 for writes in BLK5 & BLK2 and bank 1 for BLK3 & BLK1. RAM1,2,3 is also writeable.

RAM2 Mode

This mode is selected by setting the top 3 bits of the mode register to %110. All writes are targeted at bank 1 of the RAM device, reads go to either bank 1 or 2 depending on the value of a block-specific bit in the bottom of the mode register and the address the block is in.

Bit	Block	Effect
4	BLK5	0 – bank 1, 1 – bank 2
3	BLK3	0 – bank 1, 1 – bank 2
2	BLK2	0 – bank 1, 1 – bank 2
1	BLK1	0 – bank 1, 1 – bank 2

Bit 0 of the mode register controls write access to RAM1,2,3. If the bit is set the region is write-protected.

For example, setting the mode register to %11000111 selects bank 2 for reads in BLK2 & BLK1 and bank 1 for BLK5 & BLK3. RAM1,2,3 is read-only.

RAM/ROM Mode

This mode is selected by setting the top 3 bits of the mode register to %011. Writes are targeted at the RAM device to either bank 1 or 2 depending on the value of a block-specific bit in the bottom of the mode register and the address the block is in. Reads come from a fixed bank of either device depending on the same bit value as for writes.

Bit	Block	Write Effect	Read Effect
4	BLK5	0 – bank 1, 1 – bank 2	0 – RAM bank 1, 1 – EEPROM bank 0
3	BLK3	0 – bank 1, 1 – bank 2	0 – RAM bank 1, 1 – EEPROM bank 0
2	BLK2	0 – bank 1, 1 – bank 2	0 – RAM bank 1, 1 – EEPROM bank 0

1	BLK1	0 – bank 1, 1 – bank 2	0 – RAM bank 1, 1 – EEPROM bank 0

Flash Mode

This mode is selected by setting the top 3 bits of the mode register to %001. All reads and writes are targeted at the EEPROM device and the bank is determined by the bottom 4 bits of the mode register.

This is the only mode that allows writing to the EEPROM device. Modifications cannot be made by simply writing to an address as the underlying flash memory must be first erased. The device is divided into 8 sectors, an individual sector can be erased or the entire device.

Warning! A single sector maps on to two banks (e.g. sector 0 covers banks 0 & 1).

To erase a single sector the appropriate bank must first be set in the bottom of the mode register then the following sequence of writes must be performed:

- $AA →$2555
- $55 →$22AA
- $80 →$2555
- $AA →$2555
- $55 →$22AA
- $30 →any block

To erase the entire device the last write should be replaced with

- $10 →$2555

The erase operation is asynchronous, progress can be checked by

repeatedly reading the same memory location. If bit 6 inverts between reads the operation is still in progress. See the datasheet for more details, including how errors are signalled.

To write a new value to an address the appropriate bank must first be set in the bottom of the mode register then the following sequence of writes must be performed:

- $AA →$2555
- $55 →$22AA
- $A0 →$2555

followed by a write of the new value at a specific address. Completion of the operation must be checked as described above for erase. The entire sequence must be done for each byte to write.

Start Mode

On system power on, and following a cartridge reset, both registers contain %00000000. This places the FE3 in start mode, setting the following behaviour

- reads from BLK5 are targeted at bank 0 of the EEPROM device
- RAM1,2,3 and all other blocks are disabled
- the register lock bit is set

When the register lock bit is set read & write operations to the mode & resource registers have no effect.

The register lock bit is cleared on any write to an address in BLK5. Once this is done another mode can be set by writing to the mode register. The register lock bit is also set on any read to an address in BLK5.

Appendix – Quick Reference

Memory Map

The RAM and EEPROM devices occupy separate 19-bit address spaces.

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bank				Base		Offset												

Base

A14	A13	Region
0	0	RAM1,2,3
0	0	BLK1
0	1	BLK2
1	0	BLK3
1	1	BLK5

Register Descriptions

Two eight bit registers control the mapping of the RAM and EEPROM devices into the VIC-20 memory address space.

All registers are initialized to zero at power on.

The register lock bit is set at power on.

Registers are accessible if both

- the lock bit is clear
- bit 7 of the resource register is clear

Mode register $9C02

7	6	5	4	3	2	1	0
Mode			Bank/Parameter				

Mode

000	Start mode
010	Super ROM mode
100	RAM 1 mode
110	RAM 2 mode
101	Super RAM mode
011	RAM/ROM mode
001	Flash mode

Start Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	-	-	-	-
BLK1	-	-	RAM Bank 1	-
BLK2	-	-	RAM Bank 1	-
BLK3	-	-	RAM Bank 1	-
BLK5	EEPROM Bank 0	-	RAM Bank 1	-

Any write to an offset in BLK5 clears the register lock bit.

Any read from an offset in BLK5 sets the register lock bit.

Super ROM Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	RAM Bank 0	-	RAM Bank 0	-
BLK1	EEPROM	Bank $b_3b_2b_1b_0$	RAM Bank 1	-
BLK2	EEPROM	Bank $b_3b_2b_1b_0$	RAM Bank 1	-
BLK3	EEPROM	Bank $b_3b_2b_1b_0$	RAM Bank 1	-
BLK5	EEPROM	Bank $b_3b_2b_1b_0$	RAM Bank 1	-

RAM 1 Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	RAM Bank 0	-	RAM Bank 0	b_0 – write protect
BLK1	RAM Bank 1	-	RAM	b_1 – 0 = Bank 1, 1 = Bank 2
BLK2	RAM Bank 1	-	RAM	b_2 – 0 = Bank 1, 1 = Bank 2
BLK3	RAM Bank 1	-	RAM	b_3 – 0 = Bank 1, 1 = Bank 2
BLK5	RAM Bank 1	-	RAM	b_4 – 0 = Bank 1, 1 = Bank 2

RAM 2 Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	RAM Bank 0	-	RAM Bank 0	b_0 – write protect
BLK1	RAM	b_1 – 0 = Bank 1, 1 = Bank 2	RAM Bank 1	-
BLK2	RAM	b_2 – 0 = Bank 1, 1 = Bank 2	RAM Bank 1	-
BLK3	RAM	b_3 – 0 = Bank 1, 1 = Bank 2	RAM Bank 1	-
BLK5	RAM	b_4 – 0 = Bank 1, 1 = Bank 2	RAM Bank 1	-

Super RAM Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	RAM Bank 0	-	RAM Bank 0	-
BLK1	RAM	Bank $b_3b_2b_1b_0$	RAM	Bank $b_3b_2b_1b_0$
BLK2	RAM	Bank $b_3b_2b_1b_0$	RAM	Bank $b_3b_2b_1b_0$
BLK3	RAM	Bank $b_3b_2b_1b_0$	RAM	Bank $b_3b_2b_1b_0$
BLK5	RAM	Bank $b_3b_2b_1b_0$	RAM	Bank $b_3b_2b_1b_0$

RAM/ROM Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	RAM Bank 0	-	RAM Bank 0	b_0 – write protect
BLK1	RAM/EEPROM	b_1 – 0 = RAM Bank 1, 1 = EEPROM Bank 0	RAM	b_1 – 0 = Bank 1, 1 = Bank 2
BLK2	RAM/EEPROM	b_2 – 0 = RAM Bank 1, 1 = EEPROM Bank 0	RAM	b_2 – 0 = Bank 1, 1 = Bank 2
BLK3	RAM/EEPROM	b_3 – 0 = RAM Bank 1, 1 = EEPROM Bank 0	RAM	b_3 – 0 = Bank 1, 1 = Bank 2
BLK5	RAM/EEPROM	b_4 – 0 = RAM Bank 1, 1 = EEPROM Bank 0	RAM	b_4 – 0 = Bank 1, 1 = Bank 2

Flash Mode

Region	Reads from	Read control	Writes to	Write control
RAM1,2,3	-	-	-	-
BLK1	EEPROM	Bank $b_3b_2b_1b_0$	EEPROM	Bank $b_3b_2b_1b_0$
BLK2	EEPROM	Bank $b_3b_2b_1b_0$	EEPROM	Bank $b_3b_2b_1b_0$
BLK3	EEPROM	Bank $b_3b_2b_1b_0$	EEPROM	Bank $b_3b_2b_1b_0$
BLK5	EEPROM	Bank $b_3b_2b_1b_0$	EEPROM	Bank $b_3b_2b_1b_0$

Resource register $9C03

7	6	5	4	3	2	1	0
e	a	b	5	3	2	1	r

e – Register disable

0	Registers enabled
1	Registers disabled

ab – Invert address lines

a	Invert A14
b	Invert A13

5 – BLK5 disable

0	BLK5 enabled
1	BLK5 disabled

3 – BLK3 disable

0	BLK3 enabled
1	BLK3 disabled

2 – BLK2 disable

0	BLK2 enabled
1	BLK2 disabled

1 – BLK1 disable

0	BLK1 enabled
1	BLK1 disabled

r – RAM1,2,3 disable

0	RAM1,2,3 enabled
1	RAM1,2,3 disabled